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EXAMINER	
WANG, JIN CHENG	

ART UNIT	PAPER NUMBER
2672	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,354	MCCABE, DANIEL H.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-22,24,25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-22,24,25 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/06/2004 has been entered. Claims 1, 12, 20, 22, and 28 have been amended. Claims 2, 23, and 26 have been canceled. Claims 1, 3-22, 24-25, 27-29 are pending in the application.

Response to Arguments

Applicant's arguments filed Dec. 06, 2004 have been fully considered but are moot in view of the new ground(s) of rejection.

In regard to the claim 1, Duluk teaches a system for identifying pixels inside a graphics primitive of a raster image, the system comprising: A memory for storing a raster image (e.g., figures 1-12) and a graphics engine coupled to the memory and comprising a pipeline structure configured for both sequential and parallel processing (*e.g., Sequential processing includes the processing by the logic circuits such as Subrasterizer 9052, Column Selection 9054 and Sample Z Buffer 9055 and parallel processing includes the parallel sample state machines 9057; See Figures 12-14; column 37*), the pipeline structure comprising a first plurality of sequential logic circuits in series (*Duluk teaches a pipeline structure having the sequential processing including the sequential logic circuits formed by the circuit blocks such as Subrasterizer 9052, Column*

Selection 9054 and Sample Z Buffer 9055; See Figures 12-14; column 37. The circuit blocks are logic circuits that perform a sequential processing in the pipeline and therefore are called sequential logic circuits. Duluk also teaches the parallel logic circuits formed by the parallel Z Cull Sample State Machines 9057 which accesses the z values for all 16 sample points in a stamp in parallel and also computes the new primitive's z values at those sample points in parallel. See Figures 12-14; 'column 37) and a second plurality of parallel logic circuits (*e.g., parallel logic circuits formed by the parallel Z Cull Sample State Machines 9057; See Figures 12-14; column 37*) coupled to the first plurality of sequential logic circuits, each of the logic circuits configured to determine whether a polygonal portion of the raster image is at least partly inside the graphics primitive (*e.g., column 30 and 37*).

Although Duluk discloses a first plurality of sequential logic circuits in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits, each of the logic circuits configured to determine whether a polygonal portion of the raster image is at least partly inside the graphics primitive, Duluk is silent to "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image".

Bowen has taught a graphics pipeline structure comprising a first plurality of sequential logic circuits coupled in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits, each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image", (e.g., Fig. 1-3, column 3, line 60 to column 6, line 22).

It would have been obvious to one of ordinary skill in the art to have combined the pipeline structure having the multiple sequential and parallel logic circuits of Bowen with Duluk in such a manner that each individual pipeline Bowen would have been the same as the pipeline of Duluk so that the combined pipeline structure as presented in Bowen's Figs. 1 and 3 would have so produced to determine whether the received polygonal portion is at least partly inside the graphics primitive because Duluk's pipeline is configured to determine whether the received polygonal portion is least partly inside the graphics primitive (Duluk *Figures 12-14; column 37).*

Moreover, the combined pipeline structure would be the same as what has been claimed, i.e., the combined pipeline structure of Bowen and Duluk comprises a first plurality of sequential logic circuits coupled in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits (Bowen Fig. 1-3, column 3, line 60 to column 6, line 22 and Duluk *Figures 12-14; column 37),* each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image (Bowen Fig. 1-3, column 3, line 60 to column 6, line 22) and to determine whether the received polygonal portion is at least partly inside the graphics primitive (Duluk *Figures 12-14; column 37).*

One of the ordinary skill in the art would be motivated to have used a different pipeline structure having the multiple sequential and parallel logic circuits for improving the speed of the rendering process using multiple graphics pipeline (Bowen column 1, lines 40-48).

With regards to the claim 28 and similar claims such as the claims 12, 20 and 22, applicant argues that Greene does not explicitly or implicitly teach, or suggest, "a coordinate reference frame of a tile in the raster image, the coordinate reference frame located at a

geometric center of the tile." The Examiner asserts that Greene teaches a reference frame of a tile in the raster image, the coordinate reference frame located at a geometric center of a tile.

For example, in Figure 2, Greene teaches the reference frame can be selected for all the tiles as the coordinate frame for one of the tiles. Based on the selected reference frame, a coordinate transformation for the tiles can then be performed. Greene teaches that the coordinate reference frame (x', y') for the unnamed small tile on the left of the same size tile, i.e., the tile 220, wherein the origin of the coordinate reference frame (x', y') is the geometric center of the tile 212. Therefore, there is a coordinate reference frame in Fig. 2 of Greene wherein the origin of the coordinate reference frame is the geometric center of the tile 212. Therefore, Green discloses a coordinate reference frame of a tile 212 in the raster image, the coordinate reference frame located at a geometric center of the tile 212.

In another non-limiting example, Greene discloses in Figures 2 and 15 the coordinate transformation between the reference frame (x', y') of a small tile such as the tile on the left hand side of the tile 220 and the reference frame (x, y) of a big tile such as the tile 212. Such transformation can also be made between the coordinate frame (x, y) for the tile 210 and the coordinate frame (x', y') for any of the small tiles inside the tile 210. Therefore, Greene teaches in Figures 2 and 15 and column 22 the coordinate transformation between the coordinate frame (x, y) of the tile 210 and the coordinate frame (x', y') of the unnamed small tile on the left of the tile 220 as marked in Figure 15. Figure 2 also shows an origin of a coordinate reference frame of a small tile being the geometric center of the tile 212 that contains the small tile.

Greene is capable to determining or selecting the reference frame of any tile inside the big tile so that the coordinates can be transformed between the reference frame (x', y') of the

small tile and that (x, y) of the big tile (column 22). Although the origins of some of the reference frames are not exactly the geometric center of the other tiles, it is found that there is a reference frame (x', y') in the Greene's Figures and its origin is the geometric center of the tile 212 in Figure 2 or the tile 210 of Figure 15. This fact alone is sufficient to meet the claim limitation of "the geometric center" as set forth in the Claim 28.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 28-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Greene et al. U.S. Patent No. 6,480,205 (hereafter Greene).

Claim 28:

Greene teaches a method of rasterizing a graphics primitive for a raster image, the method comprising the steps of:

Deriving edge functions for the graphics primitive (e.g., column 17-19) according to a coordinate reference frame of a tile in the raster image, the coordinate reference frame located at a

geometric center of the tile in the raster image (*Figures 2 and 15 and column 22*), each edge function corresponding to an edge of the graphics primitive (column 17-22); and

Evaluating each edge function on at least one vertex (*corner of the cell*) of the tile to determine at least one vertex of the tile inside the graphics primitive (*e.g., column 17-18*).

The Examiner asserts that Greene teaches a reference frame of a tile in the raster image, the coordinate reference frame located at a geometric center of a tile.

For example, in Figure 2, Greene teaches the reference frame can be selected for all the tiles as the coordinate frame for one of the tiles. Based on the selected reference frame, a coordinate transformation for the tiles can then be performed. Greene teaches that the coordinate reference frame (x', y') for the unnamed small tile on the left of the same size tile, i.e., the tile 220, wherein the origin of the coordinate reference frame (x', y') is the geometric center of the tile 212. Therefore, there is a coordinate reference frame in Fig. 2 of Greene wherein the origin of the coordinate reference frame is the geometric center of the tile 212. Therefore, Green discloses a coordinate reference frame of a tile 212 in the raster image, the coordinate reference frame located at a geometric center of the tile 212.

In another non-limiting example, Greene discloses in Figures 2 and 15 the coordinate transformation between the reference frame (x', y') of a small tile such as the tile on the left hand side of the tile 220 and the reference frame (x, y) of a big tile such as the tile 212. Such transformation can also be made between the coordinate frame (x, y) for the tile 210 and the coordinate frame (x', y') for any of the small tiles inside the tile 210. Therefore, Greene teaches in Figures 2 and 15 and column 22 the coordinate transformation between the coordinate frame

(x, y) of the tile 210 and the coordinate frame (x', y') of the unnamed small tile on the left of the tile 220 as marked in Figure 15. Figure 2 also shows an origin of a coordinate reference frame of a small tile being the geometric center of the tile 212 that contains the small tile.

Greene is capable to determining or selecting the reference frame of any tile inside the big tile so that the coordinates can be transformed between the reference frame (x', y') of the small tile and that (x, y) of the big tile (column 22). Although the origins of some of the reference frames are not exactly the geometric center of the other tiles, it is found that there is a reference frame (x', y') in the Greene's Figures and its origin is the geometric center of the tile 212 in Figure 2 or the tile 210 of Figure 15. This fact alone is sufficient to meet the claim limitation of "the geometric center" as set forth in the Claim 28.

Claim 29:

The claim 29 encompasses the same scope of invention as that of claim 28 except additional claimed limitation of evaluating at least one edge function on at least one vertex of the tile to determine whether a portion of the tile is outside the graphics primitive; dividing the tile into subtiles if a portion of the tile is inside the graphics primitive and a portion of the tile is outside the graphics primitive; and dividing each subtile larger than a pixel and having a portion inside the graphics primitive and a portion outside the graphics primitive into subtiles. However, Greeme further discloses the claimed limitation of evaluating at least one edge function on at least one vertex of the tile to determine whether a portion of the tile is outside the graphics primitive (e.g., column 17-18); dividing the tile into subtiles if a portion of the tile is inside the graphics primitive and a portion of the tile is outside the graphics primitive (Figures 2 and 15); and

dividing each subtile larger than a pixel and having a portion inside the graphics primitive and a portion outside the graphics primitive into subtiles (e.g., Figures 2 and 15; column 17-22).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3-4, 6-7, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk et al. U.S. Pat. No. 6,664,959 (hereinafter Duluk) in view of Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen).

5. Claim 1:

(a) Duluk teaches a system for identifying pixels inside a graphics primitive of a raster image, the system comprising:

A memory for storing a raster image (e.g., figures 1-12);

A graphics engine coupled to the memory and comprising a pipeline structure configured for both sequential and parallel processing (*e.g., Sequential processing includes the processing by the logic circuits such as Subrasterizer 9052, Column Selection 9054 and Sample Z Buffer 9055 and parallel processing includes the parallel sample state machines 9057; See Figures 12-14;*

column 37), the pipeline structure comprising a first plurality of sequential logic circuits in series (*Duluk teaches a pipeline structure having the sequential processing including the sequential logic circuits formed by the circuit blocks such as Subrasterizer 9052, Column Selection 9054 and Sample Z Buffer 9055; See Figures 12-14; column 37. The circuit blocks are logic circuits that perform a sequential processing in the pipeline and therefore are called sequential logic circuits. Duluk also teaches the parallel logic circuits formed by the parallel Z Cull Sample State Machines 9057 which accesses the z values for all 16 sample points in a stamp in parallel and also computes the new primitive's z values at those sample points in parallel. See Figures 12-14; column 37*) and a second plurality of parallel logic circuits (*e.g., parallel logic circuits formed by the parallel Z Cull Sample State Machines 9057; See Figures 12-14; column 37*) coupled to the first plurality of sequential logic circuits, each of the logic circuits configured to determine whether a polygonal portion of the raster image is at least partly inside the graphics primitive (*e.g., column 30 and 37*).

(b) Although Duluk discloses a first plurality of sequential logic circuits in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits, each of the logic circuits configured to determine whether a polygonal portion of the raster image is at least partly inside the graphics primitive, Duluk is silent to "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image".

(c) Bowen has taught a graphics pipeline structure comprising a first plurality of sequential logic circuits coupled in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits, each of the sequential logic circuits and each of

the parallel logic circuits configured to receive a different polygonal portion of the raster image", (e.g., Fig. 1-3, column 3, line 60 to column 6, line 22).

(d) It would have been obvious to one of ordinary skill in the art to have combined the pipeline structure having the multiple sequential and parallel logic circuits of Bowen with Duluk in such a manner that each individual pipeline Bowen would have been the same as the pipeline of Duluk so that the combined pipeline structure as presented in Bowen's Figs. 1 and 3 would have so produced to determine whether the received polygonal portion is at least partly inside the graphics primitive because Duluk's pipeline is configured to determine whether the received polygonal portion is least partly inside the graphics primitive (Duluk *Figures 12-14; column 37).*

Moreover, the combined pipeline structure would be the same as what has been claimed, i.e., the combined pipeline structure of Bowen and Duluk comprises a first plurality of sequential logic circuits coupled in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits (Bowen Fig. 1-3, column 3, line 60 to column 6, line 22 and Duluk *Figures 12-14; column 37),* each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image (Bowen Fig. 1-3, column 3, line 60 to column 6, line 22) and to determine whether the received polygonal portion is at least partly inside the graphics primitive (Duluk *Figures 12-14; column 37).*

(e) One of the ordinary skill in the art would be motivated to have used a different pipeline structure having the multiple sequential and parallel logic circuits for improving the speed of the rendering process using multiple graphics pipeline (Bowen column 1, lines 40-48).

Claim 3:

The claim 3 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the pipeline structure being configured to divide the polygonal portion into a predetermined number of polygonal sub-portions if the polygonal portion is at least partly inside the graphics primitive. However, Duluk further discloses the claimed limitation of the pipeline structure being configured to divide the polygonal portion into a predetermined number of polygonal sub-portions if the polygonal portion is at least partly inside the graphics primitive (e.g., Duluk column 30 and 37).

Claim 4:

The claim 4 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the pipeline structure determining whether the polygonal portion of the raster image is at least partly inside the graphics primitive by evaluating edge function of the graphics primitive on at least one corner vertex of the polygonal portion. However, Duluk further discloses the claimed limitation of the pipeline structure determining whether the polygonal portion of the raster image is at least partly inside the graphics primitive by evaluating edge function of the graphics primitive on at least one corner vertex of the polygonal portion (e.g. Duluk column 30 and 37).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 4 except additional claimed limitation of the edge functions being evaluated on at least one corner vertex of the polygonal portion, to determine a corner vertex of the polygonal portion being from a primitive

edge associated with the edge function in a direction toward the inside of the graphics primitive. However, Duluk further discloses the claimed limitation of the edge functions being evaluated on at least one corner vertex of the polygonal portion, to determine a corner vertex of the polygonal portion being from a primitive edge associated with the edge function in a direction toward the inside of the graphics primitive (e.g., Duluk column 29-37).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the sequential logic circuits followed by the parallel logic circuits. However, Duluk further discloses the claimed limitation of the sequential logic circuits followed by the parallel logic circuits (e.g., Duluk Figures 12-14; column 30 and 37).

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 3 except additional claimed limitation of the predetermined number of polygonal subportions being two and the pipeline structure determining the two polygonal sub-portions by determining midpoint values of two opposite sides of the polygonal portion of the raster image and using the midpoint values as vertices of the two polygonal sub-portions. However, Duluk further discloses the claimed limitation of the predetermined number of polygonal subportions being two and the pipeline structure determining the two polygonal sub-portions by determining midpoint values of two opposite sides of the polygonal portion of the raster image and using the midpoint values as vertices of the two polygonal sub-portions (e.g., Duluk Figures 12-14; column 29-37).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the pipeline structure further comprising a predetermined number of pixel engines coupled to at least some of the parallel logic circuits and configured to determine attribute values associated with each pixel. However, Duluk further discloses the claimed limitation of the pipeline structure further comprising a predetermined number of pixel engines coupled to at least some of the parallel logic circuits and configured to determine attribute values associated with each pixel (e.g., Duluk column 46-47).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Duluk et al. U.S. Pat. No. 6,664,959 (hereinafter Duluk) and Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen), in view of Greene et al. U.S. Patent No. 6,480,205 (hereafter Greene).

Claim 5:

(1) The claim 5 encompasses the same scope of invention as that of claim 4 except additional claimed limitation of each edge function of the graphics primitive being the vector function comprising both an x-component and a y-component of a vector normal to the edge function.

(2) However, Duluk and Bowen are silent to the claim limitation of each edge function of the graphics primitive being the vector function comprising both an x-component and a y-component of a vector normal to the edge function.

(3) Greene discloses the claimed limitation of each edge function of the graphics primitive being the vector function comprising both an x-component and a y-component of a vector normal to the edge function (Greene column 18).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Greene's edge function and normal vectors into Duluk and Bowen's method for determining whether the corners of the regions are within, outside, or fully inside a graphical primitive because Duluk suggests determining whether a tile within a graphics primitive (Duluk column 30) which involves calculating the left most and right most positions of the primitive in each subraster line that contains at least one sample point and therefore suggesting an obvious modification of Duluk and Bowen.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided an edge equation for determining whether a portion of tile is covered by a graphics primitive (*e.g., determining the corner of the cell wherein the plane of the polygon is nearest using the quadrant vector being normal to the polygon; see Greene column 18*).

7. Claims 8 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Duluk et al. U.S. Pat. No. 6,664,959 (hereinafter Duluk) and Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen), in view of Greene U.S. Patent No. 6,480,205 (hereinafter Greene).

Claim 8:

(1) The claim 8 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of parallel logic circuits coupled together in a pyramid structure.

(2) However, Duluk and Bowen are silent to the claim limitation of parallel logic circuits coupled together in a pyramid structure.

(3) Greene teaches a pyramid structure for processing a tile before processing other cells in the tile in hierarchical polygon tiling (Greene column 15-17).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated Greene's pyramid structure for tiling into the Duluk and Bowen's system because Duluk's State Machines are arranged in parallel and can be arranged to process the tile stack such as the pyramid of tiles (Duluk column 37) and therefore suggesting an obvious modification of Duluk and Bowen.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have changed the parallel logic circuits in a pyramid structure to corresponds to the pyramid tile stacks and to determine any visible samples on the polygon (Greene column 16).

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Duluk et al. U.S. Pat. No. 6,664,959 (hereinafter Duluk) and Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen), in view of Larson U.S. Pat. No. 6,359,623 (hereinafter Larson).

Claim 11:

(1) The claim 11 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the polygonal portion of a raster image having a width and a height, each of the width and the height having a value of a power of 2^m.

(2) Duluk and Bowen are silent to the claim limitation of the polygonal portion of a raster image having a width and a height, each of the width and the height having a value of a power of 2^m.

(3) Larson discloses the claimed limitation of the polygonal portion of a raster image having a width and a height, each of the width and the height having a value of a power of 2^m (e.g., 16 by 16 subpixels; see column 30).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated Larson's specific selection of width and height for the polygonal portions into the Duluk and Bowen's system because Duluk suggests sub-dividing the tiles and coordinate transformation (Duluk column 20) and therefore suggesting an obvious modification of Duluk and Bowen.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided a bit wise operation for coordinate transformation (Larson column 30).

9. Claims 12-22, 24-25 and 27 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Larson U.S. Pat. No. 6,359,623 (hereinafter Larson), in view of Greene et al. U.S. Patent No. 6,480,205 (hereafter Greene).

10. Claim 12:

(1) Larson teaches a method for identifying pixels inside a graphics primitive of a raster image (see the abstract, figures 6-10) comprising the steps of:

(a) Determining whether a polygonal portion of the raster image is at least partly inside the graphics primitive using a coordinate reference frame of the polygonal portion, the coordinate

reference frame located at a point of the polygonal portion (e.g., column 3, lines 5-67; column 4, lines 1-17);

(b) Dividing the polygonal portion of the raster image into a predetermined number of polygonal subportions if the polygonal portion of the raster image is at least partly inside the graphics primitive (column 11, lines 1-16);

(c) Determining whether each polygonal sub-portion of the raster image is at least partly inside the graphic primitive (column 11, lines 1-16);

(d) Further dividing the polygonal sub-portion into a predetermined number of polygonal sub-portions if the polygonal sub-portion is at least partly inside the graphics primitive and is larger than a pixel (figure 4, column 11, lines 1-16).

(2) However, Larson does not implicitly teach using a coordinate reference frame located at the reference point (x*, y*) of figure 11 which must necessarily be the same as the geometric center (point) of a region or a tile or a portion or an area corresponding to the portion of the claimed invention.

(3) Greene teaches implicitly a reference frame located at a geometric center of the tile (See Figure 2 of Greene wherein any of the reference frames can be chosen and therefore the geometric center of the tile 210 can be chosen for a reference frame of the tile located in the left of the tile 220. For example, Greene teaches in Figures 2 and 15 the translation or transformation between the coordinate frame of the tile 210 and the coordinate frame of the tile 220. It is therefore clear that Greene teaches in Figures 2 and 15 and column 22 the translation between the coordinate frame of the tile 210 and the coordinate frame of the small tile on the left of the tile 220 as can be seen in Figures 2 and 15. For the purpose of illustration, the coordinate frame

of small tile on the left of the tile 220 is designated as (x*, y*) and the origin of the coordinate frame is the geometric center of the tile 210; See Figure 2).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Greene's selection of the reference frame centering on the geometric center of the tile into Larson's method for determining whether the corners of the regions are within, outside, or fully inside a graphical primitive because Larson suggests selecting a reference frame (Larson figure 11) with a reference point that may be the geometric center of the regions (Larson column 11, lines 1-15; See figure 2 of Greene wherein the reference frame on the left side of the reference frame 224 is located at the geometric center of the tile 212) and therefore suggesting an obvious modification of Larson.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided a reference frame that permits the equations to be evaluated with shifts and adds (Greene column 21, lines 59-67; column 22, lines 1-45).

Claim 13:

The claim 13 encompasses the same scope of invention as that of claim 12 except additional claimed limitation of recursively performing (c) and (d) until no more polygonal sub-portions that are at least partly inside the graphics primitive. However, Larson further discloses the claimed limitation of recursively performing (c) and (d) until no more polygonal sub-portions that are at least partly inside the graphics primitive (figure 4, column 11, lines 1-16).

Claim 14:

The claim 14 encompasses the same scope of invention as that of claim 12 except additional claimed limitation that determining step (a) further comprises the step of receiving a plurality of values for corner vertices of the polygonal portion and arithmetic edge functions related to the graphic primitive having a coordinate reference frame located at a geometric center of the polygonal portion, the arithmetic edge function corresponding to an edge of the graphics primitive. However, Larson further discloses the claimed limitation of that determining step (a) further comprises the step of receiving a plurality of values for corner vertices of the polygonal portion and arithmetic edge functions related to the graphic primitive having a coordinate reference frame located at a geometric center of the polygonal portion, the arithmetic edge function corresponding to an edge of the graphics primitive (figure 4, column 11, lines 1-67, column 12, lines 1-67, column 13, lines 1-51).

Claim 15:

The claim 15 encompasses the same scope of invention as that of claim 14 except additional claimed limitation that the determining step (a) further comprises the step of evaluating an arithmetic edge function corresponding to an edge of the graphics primitive on at least one corner vertex of the polygonal portion to determine a corner vertex being farthest from the corresponding edge of the graphics primitive in a direction toward the inside of the graphics primitive.

However, Larson and Greene further disclose the claimed limitation that the determining step (a) further comprises the step of evaluating an arithmetic edge function corresponding to an edge of the graphics primitive on at least one corner vertex of the polygonal portion to determine a

corner vertex being farthest from the corresponding edge of the graphics primitive in a direction toward the inside of the graphics primitive (Larson figure 4, column 11, lines 1-67, column 12, lines 1-67, column 13, lines 1-51; Greene column 18).

Claim 16:

The claim 16 encompasses the same scope of invention as that of claim 15 except additional claimed limitation of the polygonal portion being at least partly inside the graphics primitive if all arithmetic edge functions evaluated being positive. However, Larson further discloses the claimed limitation of the polygonal portion being at least partly inside the graphics primitive if all arithmetic edge functions evaluated being positive (figure 4, column 11, lines 1-67, column 12, lines 1-67, column 13, lines 1-51).

Claim 17:

The claim 17 encompasses the same scope of invention as that of claim 12 except additional claimed limitation that the dividing step (b) further comprises the step of dividing the polygonal portion into two polygonal sub-portions by determining midpoint values of two opposite sides of the polygonal portion. However, Larson and Greene further disclose the claimed limitation that the dividing step (b) further comprises the step of dividing the polygonal portion into two polygonal sub-portions by determining midpoint values of two opposite sides of the polygonal portion (Larson figure 4, column 11, lines 1-67, column 12, lines 1-67, column 13, lines 1-51; Greene column 18).

Claim 18:

The claim 18 encompasses the same scope of invention as that of claim 12 except additional claimed limitation that the dividing step (b) further comprises the step of sequentially deriving two new sets of arithmetic edge functions associated with a translated coordinate reference frame located at a geometric center of a corresponding one of the polygonal sub-portions. However, Larson further discloses the claimed limitation that the dividing step (b) further comprises the step of sequentially deriving two new sets of arithmetic edge functions associated with a translated coordinate reference frame located at a geometric center of a corresponding one of the polygonal sub-portions (figure 4, column 11, lines 1-67, column 12, lines 1-67, column 13, lines 1-51).

Claim 19:

The claim 19 encompasses the same scope of invention as that of claim 12 except additional claimed limitation that the dividing step (b) further comprises the step of outputting multiple sets of information, wherein each set of information includes corner vertices of one of the polygonal subportions and a corresponding new set of derived arithmetic edge functions defining the one polygonal subportion.

However, Larson further discloses the claimed limitation that the dividing step (b) further comprises the step of outputting multiple sets of information, wherein each set of information includes corner vertices of one of the polygonal subportions and a corresponding new set of derived arithmetic edge functions defining the one polygonal subportion (figure 4, column 11, lines 1-67, column 12, lines 1-67, column 13, lines 1-51).

Claim 20:

The claim 20 encompasses the same scope of invention as that of claim 12 except additional claimed limitation of an electronic readable medium having embodied thereon a program. However, Larson further discloses the claimed limitation of an electronic readable medium having embodied thereon a program (e.g., figure 9, column 9, lines 62-67, column 10, lines 1-6, column 17, lines 1-9).

Claim 21:

The claim 21 encompasses the same scope of invention as that of claim 20 except additional claimed limitation of recursively performing (c) and (d) until no more polygonal sub-portions that are at least partly inside the graphics primitive. However, Larson further discloses the claimed limitation of recursively performing (c) and (d) until no more polygonal sub-portions that are at least partly inside the graphics primitive (figure 4, column 11, lines 1-16).

11. Claim 22:

(1) Larson teaches a method of identifying pixels inside a graphics primitive of a raster image (see the abstract, figures 6-10) comprising the steps of:

(a) Selecting a tile including a pixel (column 10, lines 42-54);

(b) Determining if a portion of the tile is within the graphics primitive (column 10, lines 55-67, column 11, lines 1-16);

(c) Dividing the tile into sub-tiles if a portion of the tile is within the graphics primitive and another portion of the tile is outside the graphics primitive (column 11, lines 1-16);

(d) Recursively dividing each sub-tile larger than a pixel having a portion within the graphics primitive and another portion outside the graphics primitive into subtiles (figure 4, column 11, lines 1-16).

(2) However, Larson is silent to the claimed limitation of defining a coordinate reference frame for the tile, the coordinate reference frame located at a geometric center of the tile.

(3) Greene implicitly teaches defining a coordinate reference frame for the tile, the coordinate reference frame located at a geometric center of the tile (*See Figure 2 of Greene wherein any of the reference frames can be chosen and therefore the geometric center of the tile 210 can be chosen for a reference frame of the tile located in the left of the tile 220. For example, Greene teaches in Figures 2 and 15 the translation or transformation between the coordinate frame of the tile 210 and the coordinate frame of the tile 220. It is therefore clear that Greene teaches in Figures 2 and 15 and column 22 the translation between the coordinate frame of the tile 210 and the coordinate frame of the small tile on the left of the tile 220 as can be seen in Figures 2 and 15. For the purpose of illustration, the coordinate frame of small tile on the left of the tile 220 is designated as (x*, y*) and the origin of the coordinate frame is the geometric center of the tile 210; See Figure 2*).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Greene's selection of the reference frame centering on the geometric center of the tile into Larson's method for determining whether the corners of the regions are within, outside, or fully inside a graphical primitive because Larson suggests selecting a reference frame (figure 11) with a reference point that may be the geometric center of the regions (Larson column 11, lines 1-15) and therefore suggesting an obvious modification of Larson.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided a reference frame that permits the equations to be evaluated with shifts and adds (Greene column 18, 21, lines 59-67; column 22, lines 1-45).

Claim 24:

The claim 24 encompasses the same scope of invention as that of claim 22 except additional claimed limitation that the step of determining further comprises evaluating the tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive. However, Larson and Greene further disclose the claimed limitation that the step of determining further comprises evaluating the tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive (Larson column 10, lines 55-67; Greene column 18).

Claim 25:

The claim 25 encompasses the same scope of invention as that of claim 22 except additional claimed limitation that the step of recursively dividing further comprises determining if the sub-tile is at least partly within the graphics primitive by evaluating the sub-tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive. However, Larson and Greene further disclose the claimed limitation that the step of recursively dividing further comprises determining if the sub-tile is at least partly within the graphics primitive by evaluating the sub-tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive (Larson column 10, lines 55-67; Greene column 18).

Claim 27:

The claim 27 encompasses the same scope of invention as that of claim 20 except additional claimed limitation of the polygonal portion being a tile and the polygonal subportion being a subtile. However, Larson and Greene further disclose the claimed limitation of the polygonal portion being a tile and the polygonal subportion being a subtile (Larson column 10, lines 55-67; Greene column 18).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (703) 605-1213. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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